-- **14.** A metallization arrangement for a semiconductor structure, said metallization arrangement comprising:

a first substructure plane;

a second metallization plane having a first interconnected and a second interconnect separated from said first interconnect by an interspace;

a first intermediate dielectric for providing electrical insulation between said first substructure plane and said second metallization plane;

a wall forming a via hole through said intermediate dielectric, said via hole connecting said first substructure plane and said second metallization plane and being filled with a conductive material;

a liner layer made of a dielectric material, said liner layer being disposed between said second metallization plane and said first substructure plane, and being interrupted by said interspace that separates said first interconnect and said second interconnect.

15. The metallization arrangement as claimed in claim **14**, wherein said first substructure plane comprises a first metallization plane.

16. The metallization arrangement as claimed in claim **15**, wherein said first metallization plane comprises ALCu.

17. The metallization arrangement as claimed in claim **15**, wherein said second metallization plane comprises ALCu.

18. The metallization arrangement as claimed in claim **14**, further comprising a second intermediate dielectric occupying at least a portion of said interspace.

19. The metallization arrangement as claimed in claim **14**, wherein said semiconductor structure comprises an electrical circuit integrated in a silicon substrate.

20. The metallization arrangement as claimed in claim **14**, wherein said liner layer comprises a material selected from the group consisting of silicon dioxide and silicon nitride.

21. A method for fabricating a metallization arrangement for a semiconductor structure, said method comprising:

providing a first substructure plane on said semiconductor structure;

providing a first intermediate dielectric on said first substructure plane;

providing a liner layer made of a dielectric material on said first substructure plane;

providing via holes in said first intermediate dielectric and said liner layer, said via holes being filled with a conductive material, thereby completing a first resulting structure;

providing a second metallization plane on said first resulting structure;

patterning a first interconnect in said second metallization plane;

patterning a second interconnect in said second metallization plane;

interrupting said liner layer between said first interconnect and said second interconnect, thereby forming an interspace between said first and second interconnects.

22. The method as claimed in claim **21**, wherein patterning and interrupting are carried out in a common etching step.

23. The method as claimed in claim **21**, further comprising providing an electrical circuit integrated into a silicon substrate.

24. The method as claimed in claim **23**, wherein providing a liner layer comprises fabricating said liner layer from a material selected from the group consisting of silicon dioxide and

silicon nitride.

25. The method as claimed in claim **24**, wherein said patterning is carried out in a first metal etching step and said interrupting is carried out in a second silicon dioxide etching step.

26. The method as claimed in claim **21**, further comprising providing a dielectric in said interspace.

27. The method as claimed in claim **21**, further comprising providing mask on said second metallization plane for use in patterning and interrupting. --